TITLE OF THE INVENTION

METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is based upon and claims the benefit of priority from the prior Japanese Patent Applications No. 2000-320680, filed October 20, 2000; No. 2001-098182, filed March 30, 2001; No. 2001-098183, filed March 30, 2001; and No. 2001-321448, filed October 19, 2001, the entire contents of all of which are incorporated herein by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a method of manufacturing a semiconductor device. More particularly, the present invention relates to a method of manufacturing a semiconductor device having an insulation film formed by a coating technique.

2. Description of the Related Art

As wiring dimensions are changing smaller with a miniaturization of a semiconductor element, a parasitic capacity is increasing. In recent years, an increase in inter-wiring capacity of such type have a great effect on an operating speed of the device.

Conventionally, a silicon oxide film formed by a thermal CVD or plasma CVD has been employed as an interlayer insulation film of the semiconductor device. However, in recent years, in order to reduce an

interlayer capacity, it is required to apply a low permittivity film such as an organic silicon oxide film or an organic film without silicon to the interlayer insulation film.

A relative dielectric constant of a general silicon oxide film ($P-SiO_2$) obtained by conventional plasma CVD is about 4.1. In addition, the relative dielectric constant of a silicon oxide film obtained by adding fluorine (F) to the silicon oxide film ($P-SiO_2$) is 3.3. This is a lowest limit of the relative dielectric constant of the insulation film formed by the thermal CVD or plasma CVD.

In contrast, an interlayer insulation film with about 2.4 to 2.8 in relative dielectric constant can be achieved by using a low relative dielectric constant film such as the organic silicon oxide film. However, in actuality, there are a variety of problems in practical use of these low relative dielectric constant films. As one of such serious problems, there can be exemplified a lower mechanical strength of the film. If the mechanical strength of the film is low, a crack occurs with the film during film forming and after film forming or an exfoliation of the film occurs during a CMP process. If such the crack or exfoliation occurs, it is difficult to produce a wire with its high reliability.

Most of the low relative dielectric constant film

such as the organic silicon oxide film is formed by a process using coating. In the process, for instance, a liquid-like raw material called vanish in which a precursor of a substance comprising the low relative dielectric constant film is dissolved in solvent is applied on a substrate to be treated, and then, the liquid-like raw material is heated, thereby ensuring evaporation of a solvent volatile and bridge of the precursor. The precursor used here indicates a series of substances that is at a stage before a target product.

Now, the sequence of a process for forming an insulation film using a conventional coating technique will be specifically described below by way of example of a polymethyl siloxane film (organic silicon oxide film). An outline of the process is as follows (step "a" to "c").

Step "a": Applying of a vanish.

Step "b": Heat treatment at about 80 to 200℃ and for about one minute

Step "c": Heat treatment at about 400 to 450℃ for about 30 to 60 minutes

The above process will be described in detail. First, a vanish obtained by dissolving polymethyl siloxane in solvent is applied with a spin coating technique using a coater, and a coat film is formed (step "a"). Next, the substrate is heated at a